The following Listing of Claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A data conversion system ~~wherein~~ in which one of ~~first and second~~ a plurality of nodes on an IEEE1394 bus serves as a cycle master, ~~first data is transferred~~ transmits data from ~~the first~~ one of the plurality of nodes to ~~the second node~~ another node of the plurality of nodes in synchronism with a cycle start packet output from the cycle master, and ~~second data generated by conversion of the first~~ converts the data in the ~~second~~ other node of the plurality of nodes, ~~is synchronized with an external reference signal and output, comprising:~~ wherein

a first node of the plurality of nodes comprises an external synchronizing signal receiver for receiving an external reference signal provided on at least one of the first and second nodes, and a synchronization adjustment unit for synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal received by the external synchronizing signal receiver, and

the first node or a second node of the plurality of nodes comprises a data conversion unit for converting the data and outputting the converted data in synchronism with the reference signal.

2. (Currently Amended) The data conversion system according to claim 1, wherein ~~the first node is hardware comprising a 1394OHCI compliant IEEE1394 interface for outputting a~~ the transmitted data is a video signal in DV format ~~as first data, and the second~~

~~node is data conversion hardware for outputting~~ and the converted data is an analog video signal or SDI video signal ~~as second data.~~.

3. (Currently Amended) The data conversion system according to claim 1, wherein the ~~second~~ first node ~~comprises the external synchronizing signal receiver and synchronization adjustment unit, and~~ serves as cycle master for data transfer.

4. (Currently Amended) The data conversion system according to claim 1, wherein the ~~first~~ second node comprises the synchronization adjustment unit, ~~the second node comprises the external synchronizing signal receiver and the synchronization adjustment unit,~~ and the cycle start packet frequency is synchronized with the frequency of the reference signal received by the external synchronizing signal receiver by means of the synchronization adjustment unit of the node that serves as the cycle master.

Claims 5-7 (Cancelled)

8. (New) A device for transmitting a cycle start packet serving as a cycle master on an IEEE1394 bus and converting data transmitted from a node connected on the IEEE1394 bus in synchronism with the cycle start packet, comprising:

an external synchronizing signal receiver for receiving a reference signal;

a data conversion unit for converting the data and outputting the converted data in synchronism with the reference signal; and

a synchronization adjustment unit for synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal.

9. (New) The device according to claim 8, wherein the data converted is a video signal in DV format, and the data outputted is an analog video signal or SDI signal.

10. (New) A device for generating a cycle start packet serving as a cycle master on an IEEE1394 and transmitting data to a node connected on the IEEE1394 bus in synchronism with the cycle start packet, comprising:

an external synchronizing signal receiver for receiving a reference signal; and

a synchronization adjustment unit for synchronizing the frequency of the cycle start packet output from the cycle master with the frequency of the reference signal.